REMARKS

In the Official Action mailed on **29 April 2009**, Examiner reviewed claims 1-2, 4-11, and 13-20. Examiner rejected claims 1, 10, and 19 under 35 U.S.C. § 102(b) based on Herlihy et al. (U.S. Patent No. 5,428,761, hereinafter "Herlihy"). Examiner rejected claims 2, 4-7, 9, 11, 13-16, 18, and 20 under 35 U.S.C. § 103(a) based on Herlihy, and Rajwar et al. (U.S. Patent No. 7,120,762, hereinafter "Rajwar"). Examiner rejected claims 8 and 17 under 35 U.S.C. § 103(a) based on Herlihy, Rajwar, and Hecht et al. (U.S. Pub. No. 2003/0064808, hereinafter "Hecht").

Rejections under 35 U.S.C. 102(b)

Examiner rejected claims 1, 10, and 19 under 35 U.S.C. § 102(b) based on Herlihy. Applicant respectfully disagrees with the rejection. Herlihy nowhere discloses a store buffer that is a hardware structure separate from a register file.

Herlihy discloses a computer system which includes a CPU and a cache memory separate from the CPU.[1] The Herlihy CPU includes an internal register set.[2] When the Herlihy CPU has finished processing data for a transaction, the CPU writes the result to the cache.[3] Then, when the transaction ends, if a status bit is still set the Herlihy CPU commits the result from the cache to memory.[4] Herlihy also discloses a "store-transactional" (ST) instruction to tentatively write the value in a register to a shared memory location.[5] In other words, Herlihy discloses only an internal register set structure, and then discloses writing a value from a register to the cache and/or memory. Herlihy nowhere discloses committing store buffer entries generated during transactional execution to

1 see Herlihy, FIG. 1; also column 5, lines 28-33
2 see *id.*, column 5, lines 11-15; also, FIG. 1, unit C
3 see *id.*, column 6, lines 53-56
4 see *id.*, column 6, lines 62-68
5 see *id.*, column 8, lines 1-8

memory, wherein the store buffer is a separate structure in hardware from a register file.

In contrast, in embodiments of the present invention the processor includes a register file, and a separate store buffer.[6] For a commit operation, embodiments of the present invention commit entries from the store buffer to main memory.[7] Additionally, for a commit operation embodiments of the present invention commit register file changes.[8] In embodiments of the present invention, **the store buffer is a separate structure in hardware from the register file**.[9] Herlihy nowhere discloses committing store buffer entries generated during transactional execution to memory, wherein the store buffer is a separate structure in hardware from a register file.

Accordingly, Applicant has amended the independent claims to clarify that in embodiments of the present invention the store buffer is a separate structure in hardware from the register file. These amendments are supported in paragraphs [0051]-[0052], [0079]-[0080], and FIG. 1 of the instant application. No new matter was added. Herlihy nowhere discloses committing store buffer entries generated during transactional execution to memory, wherein the store buffer is a separate structure in hardware from a register file.

Hence, Applicant respectfully submits that independent claims 1, 10, and 19 as presently amended are in condition for allowance. Applicant also submits that the dependent claims that depend upon these independent claims are in condition for allowance and for reasons of the unique combinations recited in such claims.

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6 see instant application, FIG. 1; also, paragraphs [0051]-[0052]
7 see *id.*, paragraph [0079]; also, FIG. 7
8 see *id.*, paragraph [0080]; also, FIG. 7
9 see *id.*, FIG. 1

CONCLUSION

It is submitted that the application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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